Implementation of a Digital Watermarking Algorithm on an FPGA

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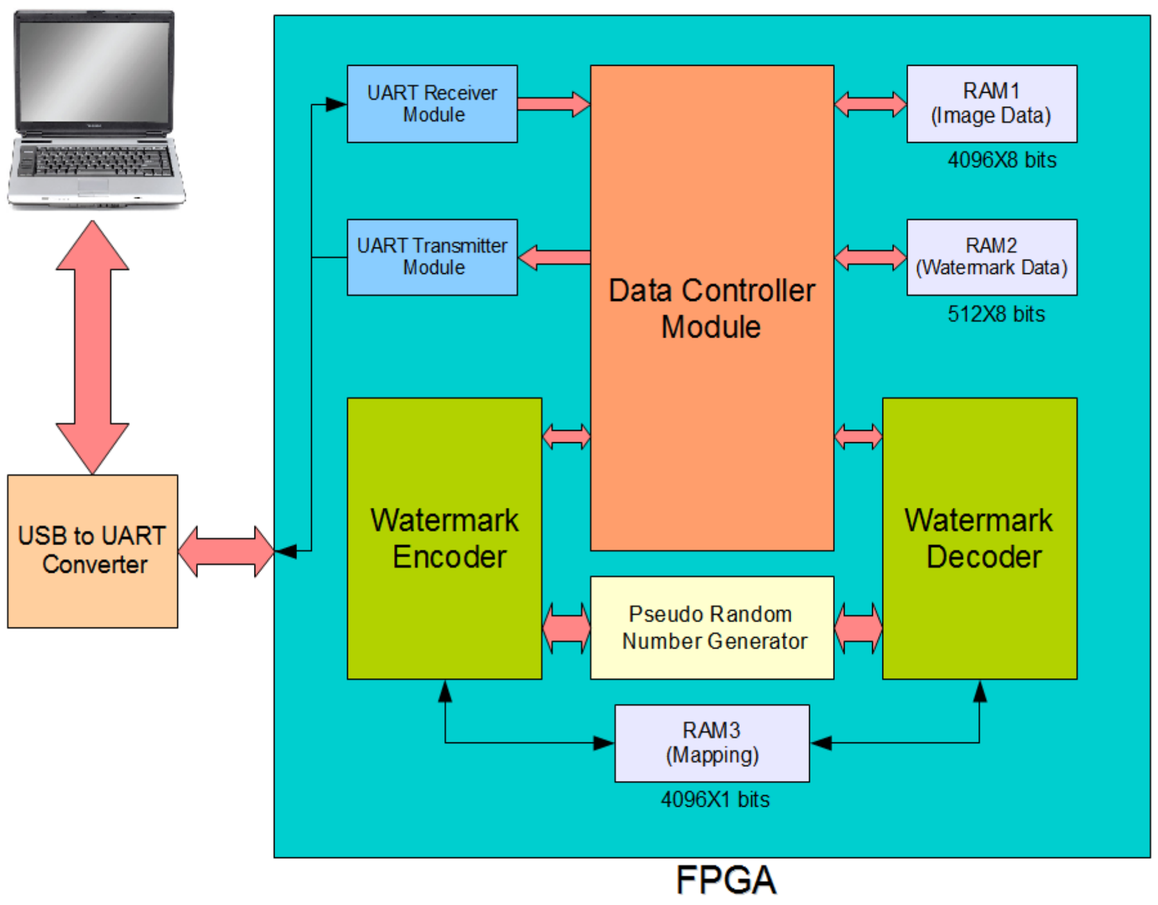
Abstract

We have implemented a digital image watermaking system on an FPGA. Watermarking is the process of hiding information inside noise tolerant mediums such as images or videos. Our design consists of modules such as the embedder, extractor, random number generator and the memory module. The system takes an image and the watermark as input from the computer along with the specifications, embeds or extracts the watermark and sends the data back to the computer.

Overview of the System

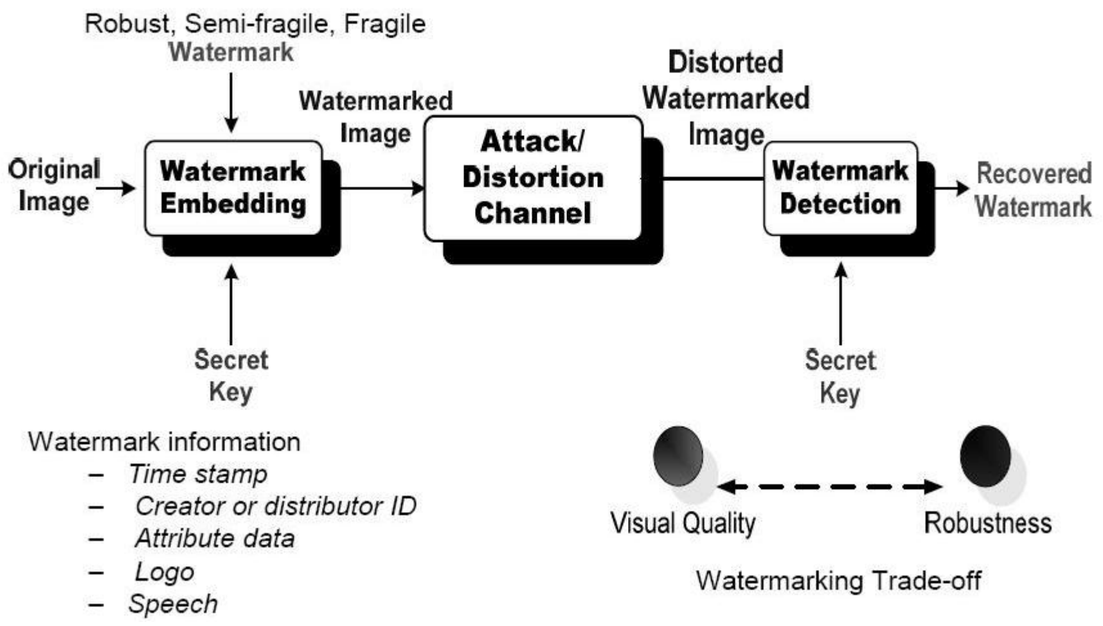


FPGA Design

Verilog HDL (a hardware description language) was used for design of the circuit. For synthesis and simulation stages Xilinx's ISE tool was used. Maximum clock frequency of 89.96 MHz was achieved for the digital circuit and 220 logic blocks were occupied after synthesis.

Main Components

- Digilent BASYS2 FPGA Board
- USB to Uart Converter



Conclusion

Performance of the algorithm on hardware is significantly better than its software counterpart. Algorithm is resistant to some attacks but considering it is a spatial domain algorithm, degree of robustness is acceptable. Although it is not possible to implement on the FPGA model we have used, with a more advanced FPGA model, the performance could be improved through parallelised hardware. We have developed the paralellised version of the design and verified it on simulation.

References:

· Intelligent Watermarking Techniques, Jeng-Shyang Pan, Hsiang-Cheh Huang, Lakhmi C. Jain. Series on Innovative Intelligence, Vol 7.

· Pan, J.S., Huang, H.C., and Wang, F.H. (2001), “Genetic watermarking techniques,” Proceedings of the Fifth International Conference on Information Engineering Systems & Allied Technologies, pp. 1032-1036.

· Verilog HDL: A guide to Digital Design and Synthesis, Samir Palnitkar, SunSoft Press, 1996.

· Various Xilinx documents and application notes.